IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

SOLAS OLED LTD., Plaintiff, v. GOOGLE LLC, Defendant.	)	Case No. 6:19-cv-00515-ADA
SOLAS OLED LTD., Plaintiff, v. APPLE INC., Defendant.	)	Case No. 6:19-cv-00537-ADA
SOLAS OLED LTD., Plaintiff, v. HP INC., Defendant.	)	Case No. 6:19-cv-00631-ADA

DEFENDANTS' AND INTERVENOR'S OPENING CLAIM CONSTRUCTION BRIEF

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DD04	Phillip A. Laplante, Comprehensive Dictionary of Electrical Engineering 213, 643 (Taylor & Francis Group, 2nd ed. 2005)
DD05	Stan Gibilisco, The Illustrated Dictionary of Electronics 179 (McGraw-Hill, 8th ed. 2001)
DD06	A Dictionary of Science 738-39 (Oxford University Press, 2006)

The Defendants and Intervenor hereby submit their Opening Claim Construction Brief.

I. U.S. Patent No. 7,446,338 ("'338 Patent")

A. '338 Patent Background

The '338 Patent is directed to active-matrix organic electroluminescent (AMOLED) display panels. *See, e.g.*, '338 at 1:17-21, 8:18-23. These are many-layered devices that consist of organic electroluminescent pixels and circuitry, which drive the pixels to produce particular colors and brightness. Figure 6 illustrates the layered structure of an exemplary display panel of the '338 Patent, consisting of two main structures: (1) the red, green, and blue OLED pixels (Pr, Pg, and Pb), each made up of a pixel electrode 20a, an electroluminescent layer 20b, and a counter electrode 20c; and (2) the layers making up the "transistor array substrate" 50, *id.* at 10:42-47, which includes the transistors 21 and 23 that make up the active-matrix circuit for each pixel:

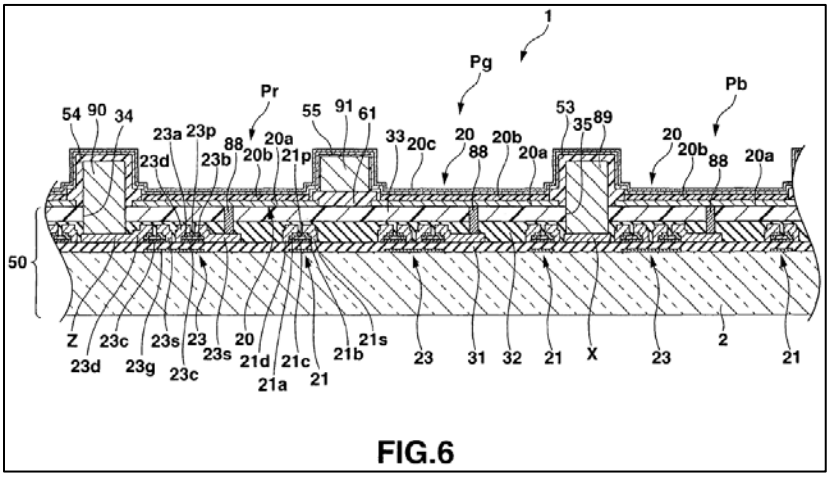


FIG.6

In the original patent application, prosecution claim 1 was directed to the arrangement of elements in the layered structure, as exemplified by Figure 6. That claim, however, was rejected as anticipated by prior art. To overcome the rejection, the applicants amended claim 1 to recite the particular three-transistor pixel circuit structure recited by a dependent claim (prosecution claim 2), illustrated in Figure 2 of the '338 Patent. Ex. AA01 at 2-3, 12. This three-transistor circuit uses a pull-out current, which the patent refers to as a write current, to set the brightness of

each individual pixel. This current-controlled structure differed from circuits that used particular voltage signal levels applied to the gate of the driving transistor, rather than current, to control pixel brightness. *See, e.g.*, '338 at 1:21-41 (describing that in a prior art reference, "a voltage of level representing the luminance is applied to the gate of the driving transistor through a signal line."). After the addition of this three-transistor circuit structure limitation, the claims of the '338 Patent were allowed.

B. "transistor array substrate" (claim 1)

Plaintiff's Proposal	Defendants' Proposal
"layered structure upon which or within which a transistor array is fabricated"	"a layered structure composed of a bottom insulating layer through a topmost layer on whose upper surface pixel electrodes are formed, which contains an array of transistors"

The term "transistor array substrate" has no customary meaning in the art. It is a term specific to the '338 Patent, which the '338 Patent defines as a layered structure composed of a bottom substrate layer through a topmost layer on whose upper surface electrodes are formed, which contains an array of transistors. *See, e.g.*, '338 at 10:45-47, cl. 1. Both the language of claim 1 and the specification support Defendants' proposal. Solas's construction, in contrast, is inconsistent with the claim language and the specification, and would leave the boundaries of the "transistor array substrate" indefinite.

1. The transistors are contained in the transistor array substrate

By the plain terms of the claim, the transistor array substrate must contain a plurality of transistors for each pixel (*i.e.*, an array of transistors). The claim language recites "a transistor array substrate which includes a plurality of pixels and comprises a plurality of transistors for each pixel, each of the transistors including a gate, a gate insulating film, a source, and a drain." '338 at 24:15-18 (emphasis added). The term "comprises" means "including but not limited to." *See, e.g., Genentech, Inc. v. Chiron Corp.*, 112 F.3d 495, 501 (Fed. Cir. 1997).

But as Solas's expert in the Eastern District of Texas litigation admitted, Solas's proposal ("layered structure upon which or within which a transistor array is fabricated") would permit the transistor array substrate to contain no transistors. *See* Ex. AA03 (Flasck Depo.) at 64:17-65:14. That is contrary to the claim language.

Moreover, the specification explains that the transistors are contained within the transistor array substrate. *See, e.g.*, '338 at 10:45-47. Thus, based on the plain claim language, and the specification's disclosures, the transistor array substrate contains an array of transistors. Solas's contrary proposal is inconsistent with the intrinsic evidence.[1]

2. The '338 Patent defines which layers of an OLED display panel constitute the "transistor array substrate"

The claim language and the specification make clear that the "transistor array substrate" is a layered structure composed of a bottom substrate layer through a topmost layer on whose upper surface pixel electrodes are formed, as Defendants propose.

The claim language strongly supports Defendants' proposal. After reciting "a transistor array substrate," claim 1 proceeds to recite (1) that the interconnections "project from a surface of the transistor array substrate" and (2) "the pixel electrodes being arrayed along the interconnections between the interconnections on the surface of the transistor array substrate." As Solas admits, the claim language provides that the pixel electrodes are "on the surface of the transistor array substrate." AA04 at 3. This means that the "transistor array substrate" constitutes the layers up to but not including the pixel electrodes, as Defendants propose.

[1] Defendants note that in the E.D. Tex. litigation, the Court found that the specification's references to a transistor array substrate containing an array of transistors did not justify including the requirement. *See* Ex. AA02 (Dkt. 99 in *Solas OLED Ltd. v. Samsung Display Co., et al*, Case No. 2:19-cv-152 (E.D. Tex. April 17, 2020) at 14. Defendants respectfully submit that the claim language is decisive that the transistor array substrate contains the transistors, as shown above.

Moreover, before the Patent Trial and Appeal Board, Solas itself agreed that "transistor array substrate" in the '338 patent should be construed as "layered structure including a bottom insulating substrate through a topmost insulating layer on whose surface the pixel electrodes are formed," as Defendants propose. Ex. AA05 at 27-28.

Consistent with the claim language and Solas's position before the PTAB, the specification discloses that the transistor array substrate constitutes the layers up to (but not including) the pixel electrode. The specification expressly states that "[t]he layered structure from the insulating substrate 2 to the planarization film 33 is called a transistor array substrate 50." '338 at 10:45-47 (emphasis added). *See, e.g., Sinorgchem Co., Shandong v. Int'l Trade Comm'n*, 511 F.3d 1132, 1136 (Fed. Cir. 2007) ("[T]he word 'is' ... may signify that a patentee is serving as its own lexicographer.") (citation and internal quotation marks omitted).

Next, the specification explains that "[t]he plurality of sub-pixel electrodes 20a are arrayed in a matrix on the upper surface of the planarization film 33, *i.e.*, the upper surface of the transistor array substrate 50."[2] '338 at 11:50-53 (emphasis added). *See Edwards Lifesciences LLC v. Cook Inc.*, 582 F.3d 1322, 1334 (Fed. Cir. 2009) ("the specification's use of '*i.e.*' signals an intent to define the word to which it refers"). This passage reiterates that the surface on which the pixel electrodes are formed constitutes the upper surface of the transistor array substrate.

All the layers beneath the pixel electrode are part of the transistor array substrate, as illustrated in Figure 6 of the patent and as described through the specification. *See, e.g.*, '338 at

[2] The Court in the E.D. Tex. litigation found that the fact that this portion of the specification referred to "transistor array substrate 50," favored "finding that this disclosure refers to a specific structure in a particular disclosed embodiment rather than to the meaning of 'transistor array substrate' in general." Ex. AA02 at 14. The specification, however, does not disclose any "transistor array substrate" other than the "transistor array substrate 50" nor suggests that one would have a different top surface. Further, as discussed above, the other claim language of claim 1 itself strongly supports Defendants' reading.

8:21-23 ("The display panel 1 is formed by stacking various kinds of layers on the insulating substrate 2 which is optically transparent."); *id.* at 10:45-47 ("The layered structure from the insulating substrate 2 to the planarization film 33 is called a transistor array substrate 50.").

Solas's construction—"layered structure upon which or within which a transistor array is fabricated"—would leave indeterminate which layers are part of the transistor array substrate and which are not. Indeed, Solas's expert in the Eastern District of Texas litigation acknowledged in deposition that, under Solas's proposal, multiple different combinations of layers in a single device could alternatively be considered to be a "transistor array substrate." Ex. AA03 (Flasck Dep. Tr.) at 69:3-11, 104:4-105:3. Under Solas's proposal, there would not even be a basis to include within the "transistor array substrate" layers that the specification expressly identifies as portions of the transistor array substrate. For instance, planarization layer 33 is neither beneath the array of transistors nor a layer that contains transistors, and would fall outside the scope of the claims under Solas's construction. Yet, the '338 patent is explicit that planarization layer 33 is part of the claimed "transistor array substrate." '338 at 11:50-53.

Thus, consistent with all of the intrinsic evidence, "transistor array substrate" should be construed as "a layered structure composed of a bottom substrate layer through a topmost layer on whose upper surface pixel electrodes are formed, which contains an array of transistors."

C. "project from a surface of the transistor array substrate" (claim 1)

Plaintiff's Proposal	**Defendants' Proposal**
"extend beyond an outer surface of the transistor array substrate"	"extend above the upper surface of the transistor array substrate"

The parties' dispute over this term concerns the boundary of the transistor array substrate from which the interconnections project. The disclosures of the '338 Patent uniformly establish

that the interconnections extend above the upper surface of the transistor array substrate, and not from a side or bottom surface of the transistor array substrate.

The specification explains that the interconnections project from the upper surface of the transistor array substrate. The specification explains "[t]he common interconnection 91 is formed by electroplating and is therefore formed to be much thicker than the signal line Y, scan line X, and supply line Z and *project upward from the surface* of the planarization film 33." '338 at 10:54-58 (emphasis added). The specification then explains that "[t]he thickness of the select interconnection 89 and feed interconnection 90 is larger than the total thickness of the protective insulating film 32 and planarization film 33 so that the select interconnection 89 and feed interconnection 90 *project upward from the upper surface* of the planarization film 33," *id.* at 11:36-41 (emphasis added), which is the upper surface of the transistor array substrate, *see, e.g.*, *id.* at 10:49-50 ("the upper surface of the planarization film 33, ***i.e.***, the upper surface of the transistor array substrate 50") (emphasis added); 11:50-52 (same); 10:45-47.

As shown in annotated Figure 6 below, the interconnections (89, 90, and 91 shown in red) all extend above the upper surface (33 shown in yellow) of the transistor array substrate:

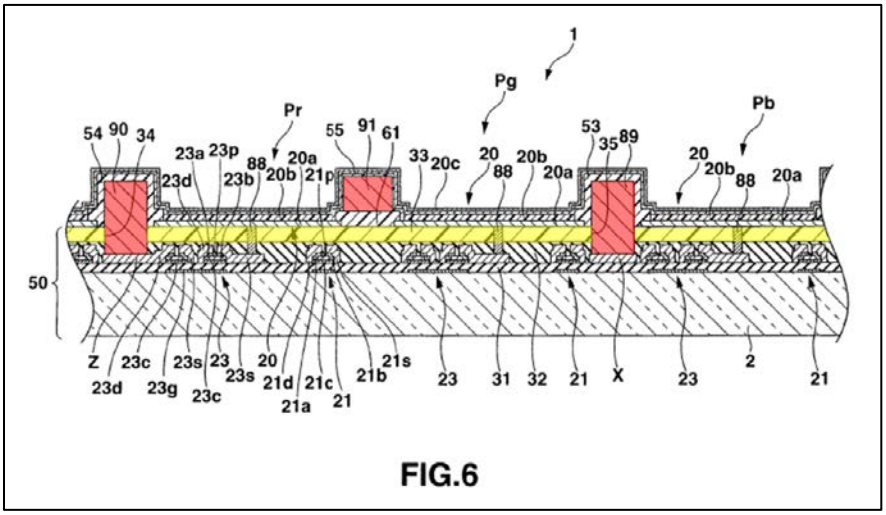


FIG.6

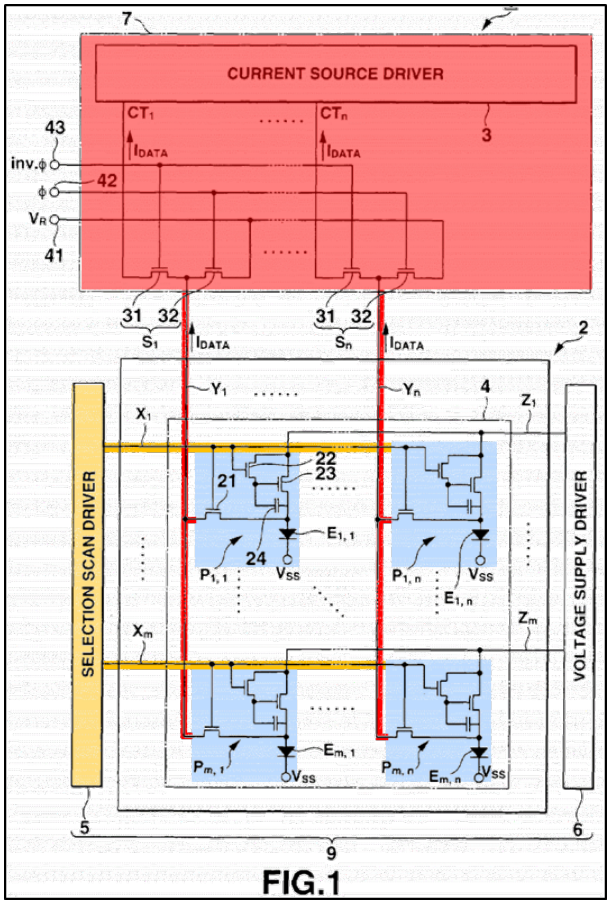
Defendants' proposal further aligns with a stated purpose of the projecting interconnections, which the '338 patent repeatedly explains is to "serve as partition walls to prevent leakage of an organic compound-containing solution." '338 at 6:24-30*; see also id.* at 6:38-42. To serve as these partition walls, the interconnections must extend past the upper surface of the transistor array substrate. This is precisely what the specification describes and its Figures illustrate. In language that parallels the claim language, the specification explains that projecting interconnections extend above the upper surface of the transistor array substrate to prevent leakage of the organic electroluminescent compound: "[t]he thick select interconnection 89, feed interconnection 90, and common interconnection 91 whose tops are much higher than that of the insulating line 61 *are formed* between the sub-pixel electrodes 20a adjacent in the vertical direction *to project* [sic] *respect to the surface of the transistor array substrate 50. Hence, the organic compound-containing solution* applied to a sub-pixel electrode 20a *is prevented from leaking* to the sub-pixel electrode 20a adjacent in the vertical direction." *Id.* at 12:62-13:3 (emphases added).

Although the Court in the Eastern District of Texas litigation declined to include the "upper" portion of Defendants' construction, stating that the term "upper" "lacks sufficiently clear meaning in the context of a "display panel" as claimed in . . . Claim 1," Ex. AA02 at 18, the '338 Patent makes the meaning of "upper" surface clear relative to the surrounding elements, *see, e.g.*, 10:54-58 & 11:36-41 (referring specifically to the "upper surface"). The upper surface is the contact between the transistor array substrate and the pixel electrodes.

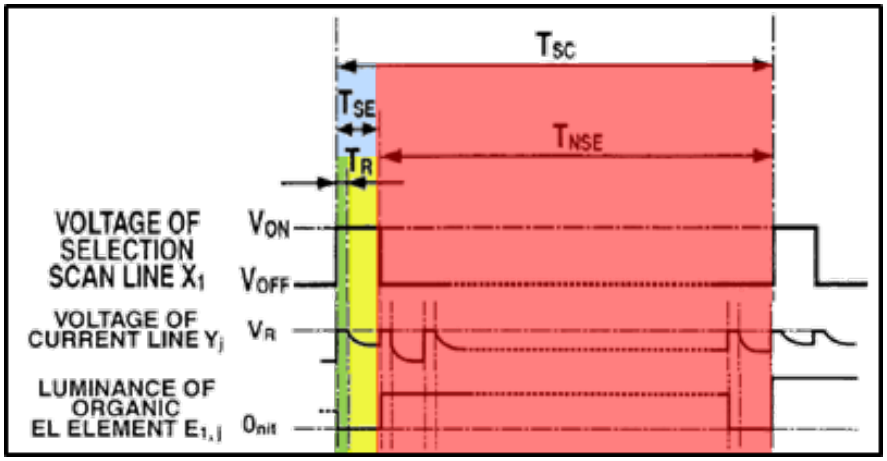
II. U.S. Patent No. 7,499,042 ("'042 Patent")

A. '042 Patent Background

The '042 Patent is directed to an OLED display panel shown in Figure 1 (annotated right). The panel includes a matrix of pixel circuits $P_{1,1}$ to $P_{m,n}$ (each circuit in blue), controlled by a selection scan driver (orange) and a data driving circuit (red). '042 at 4:19-43, 4:59-5:24. The scan driver connects to rows of pixels circuits through selection scan lines X_1-X_m (orange), with each line connecting to one row. *Id.* The data driving circuit similarly connects to columns of pixel circuits through current lines Y_1-Y_n (red), with each line connecting to one column. *Id.*



As depicted in Figure 4 (annotated), each selection scan line is turned on and selects a corresponding row of pixels in the "selection period" T_{SE} (blue) for that row. *Id.* at 4:33-38, 9:20-26. The selection period is divided into two sub-periods: (1) a reset sub-period T_R (green), when a "reset voltage" V_R is applied to the pixels of that row, followed by (2) a second sub-period (yellow) when a "designating current" I_{data} is applied. *Id.* at 11:50-57, 13:10-18. Following the selection period is a "non-selection period" T_{NSE} (red), when the selection scan line is turned off and unselects that row of pixels. *Id.* at 10:19-27.



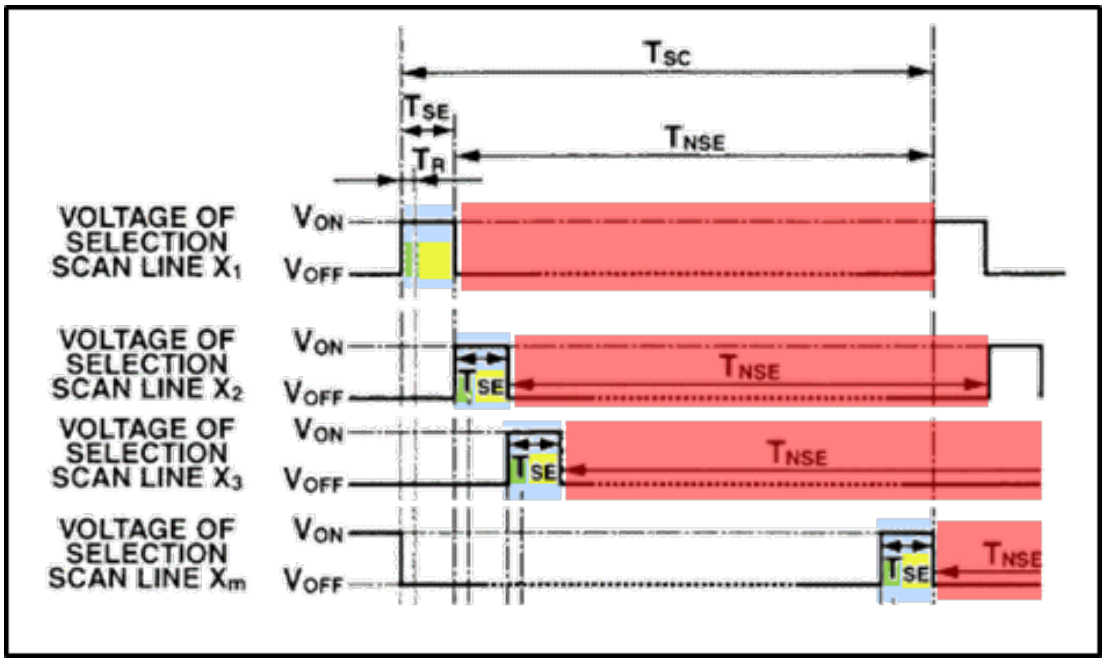
B. "selection period" (Claim 1)

Solas's Proposal	HP's Proposal
"time period during which a plurality of pixel circuits is selected"	"time duration in which a selected selection scan line is kept active"

HP's construction follows from the patent's definition of "selection period" to mean a time duration when a "selection scan line" is selected, meaning it is "active" or turned on. It also clarifies that the selected "selection scan line" is "kept" active because, otherwise, a "selection period" could encompass periods when a "selection scan line" is not kept active and is actually turned off and unselected. Yet, by not including any notion of *keeping* the selection active, Solas's proposal advances just such an expansive and contradictory understanding of "selection period" as encompassing periods when a line or circuit is inactive and not selected. Solas's proposal also contradicts the specification, which uses another term, "non-selection period," to refer to periods when a "selection scan line" is inactive. Moreover, by not tying the "selection period" to any "selection scan line," Solas's proposal disregards that the specification expressly defines a "selection period" in relation to the "selection scan line" for a *row* of pixel circuits, rather than just any "plurality of pixel circuits."

HP's construction follows from the specification's definition of a "selection period" as a time duration during which a given "selection scan line" is turned "ON": "*[a] period in which the selection scan driver 5 applies the ON voltage* V_{ON} *to the selection scan line* X_i *in the ith row* and thereby selects the selection scan line X_i in the ith row *is called a selection period* T_{SE} of the ith row." *Id.* at 9:13-32. The specification provides this definition in connection with Figure 4 (annotated below), which shows that the "selection period" T_{SE} for each selection scan line X is the time that the line is set to V_{ON} (blue). *Id.* As also shown in Figure 4, the "selection period" for each scan line X_1-X_m is divided into two sub-periods, between which the selection scan line is

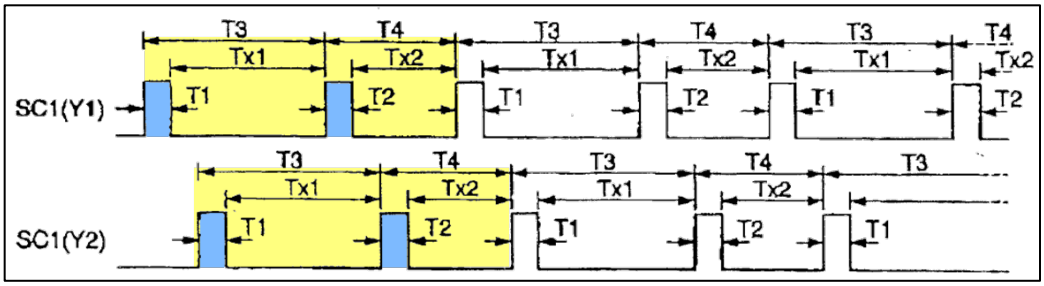
kept active. In the first sub-period, known as the reset period T_R (green), "the selection scan driver 5 *applies the ON voltage* V_{ON} *to the selection scan line* X_i." *Id.* at 13:10-18. In the second sub-period, a tone designating current I_{DATA} is applied to the current lines (yellow). *Id.* at 13:55-64. Notably, "after the reset period T_R in the selection period T_{SE} of the ith row, the selection scan driver 5 *keeps applying the ON voltage* V_{ON} *to the selection scan line* X_i." *Id.* A "selection period" thus refers to when a "selection scan line" for a row of pixel circuits is active and turned on.



The specification precludes the possibility that the "selection period" for a row of pixel circuits could encompass a time duration when a corresponding "selection scan line" is inactive or off. First, as described above, the specification states that the circuit "*keeps* applying the ON voltage V_{ON} to the selection scan line X_i" between the two sub-periods of the "selection period." *Id*. Second, the specification defines the time when "selection scan line" is inactive or "OFF" using another term, a "*non-selection period*": "*a period in which the selection scan driver 5 applies the OFF voltage* V_{OFF} to the selection scan line X_i in the ith row and thereby keeps the selection scan line X_i in the ith row unselected *is called a non-selection period* T_{NSE} of the ith row." *Id.* at

9:49-57. In Figure 4 (above), the non-selection period T_{NSE} (red) of every selection scan line X_1 to X_m corresponds to when that line is set to V_{OFF}.

Further, statements made in prosecution of a related foreign counterpart patent are relevant to construing claims of a U.S. patent. *E.g., Glaxo Grp. Ltd. v. Ranbaxy Pharm., Inc.*, 262 F.3d 1333, 1337 (Fed. Cir. 2001). During prosecution of a European counterpart to the '042 Patent, European Patent No. 1,714,266 ("EP '266"), the applicants argued that a "selection scan line" has to be kept active during the entire "selection period" to distinguish discontinuous selection periods in prior art European Patent Application No. 1,372,136 ("EP '136").[3] *See* Ex. BB01 at DEFS_CC_0510-0511. As shown in its Figure 4 (annotated below), in EP '136, each selection scan line, SC1(Y1) and SC1(Y2), is selected and active in two separate periods T1 and T2 (blue) in each frame period (yellow). Based on this disclosure, the applicants argued that EP '136 "carries out the reset and the writing process in *different selection periods*, while the present invention carries out these processes in the *same selection period*." *Id.*; Ex. BB02 at DEFS_CC_0997.



The applicants contrasted EP '136 with the '042 Patent, where "*each selection[] scan line[] is selected once and not twice* in a frame period," which leads to "significantly reduced" "power consumption." *Id.* Thus, the applicants relied on their alleged invention having one "selection period," during which the "selection scan line" is kept active, to distinguish prior art having two discontinuous selection periods separated by a period when the selection scan line is inactive.

[3]The applicants submitted EP '136 in an Information Disclosure Statement to the PTO during the '042 Patent prosecution, acknowledging its relevance to the '042 Patent. *See* Ex. BB02 at DEFS_CC_0975, 0977.

Solas's proposal of "time period during which a plurality of pixel circuits is selected" is incorrect for several reasons. First, it severs any connection between the "selection period" and "selection scan line." But as excerpted above, the specification expressly defines the "selection period" in relation to whether a corresponding "selection scan line" is active or turned on. '042 at 9:20-36. Second, by severing the connection, Solas's proposal is overbroad and ambiguous as to which "plurality of pixel circuits is selected." In each "selection period," a "selection scan line" and corresponding *row* of pixel circuits is active and selected. Solas's proposal, however, allows the selection of *any* pixel circuits, regardless of their arrangement. But there is no enabling disclosure for selecting a column, diagonal line, or any random grouping of pixel circuits during any "selection period." Third, by not including any notion of *keeping* the selection active during the "selection period," Solas's proposal encompasses periods when the "selection scan line" is at least temporarily inactive or *not* selected. Solas's proposal that a "selection period" could mean a duration when a line or circuit is un-selected contradicts both the plain meaning of "selection period" and the specification's usage of "*non*-selection period" to refer to such a duration.

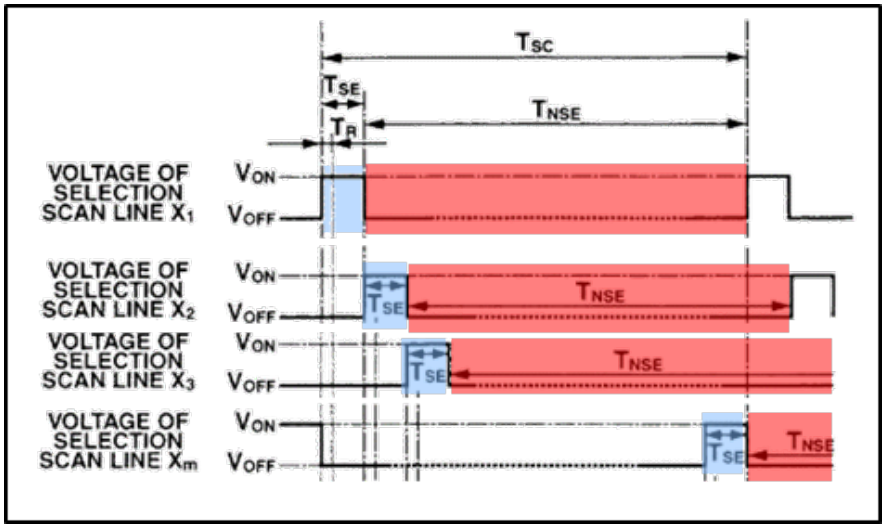
C. "sequentially selects said plurality of selection scan lines in each selection period" (Claim 1)

Solas's Proposal	HP's Proposal
Plain and ordinary meaning	"selects said plurality of selection scan lines one per each of a plurality of non-overlapping selection periods"

As discussed in Section II.A ('042 Patent Background) and with respect to Figure 1, the '042 Patent discloses rows of selection scan lines, with each row selected during a corresponding "selection period." HP proposes to construe this "sequentially . . ." term to clarify that the "selection periods" for different "selection scan lines" must be "non-overlapping" in time. This follows from express statements made in the specification and the fundamental operation of OLED circuits. Solas's "plain and ordinary meaning" proposal fails because, as an initial matter, the

disputed term is a lengthy, technical phrase lacking any plain and ordinary meaning. It also fails to the extent Solas contends that "selection periods" for different selection scan lines can overlap.

The '042 Patent specification is clear: "*the selection periods T_{SE}* of the selection scan lines X_1 to X_m *do not overlap each other*." '042 at 9:29-31. The specification explains why this statement is true. It states that each selection scan line is controlled by the same "selection scan driver," which the patent described as a "shift register" that "*individually applies*, to the selection scan lines X1 to Xm, *a high-level (ON-level) ON voltage VON*," as shown in Figure 4 (annotated). *Id.* at 9:13-19. This figure also shows that the "selection period" T_{SE} for any one selection scan line (blue) occurs only during the non-selection periods T_{NSE} of the other selection scan lines (red).



The specification confirms this, stating: "*while applying the ON voltage V_{ON} to the selection scan line X_i, the selection scan driver 5 applies the OFF voltage V_{OFF} to the other selection scan lines* X_1 to X_m (except for the selection scan line X_i)." *Id.* at 9:26-29. Thus, at any given time, only one selection scan line can be selected and active during its "selection period," meaning that the "selection periods" of all the selection scan lines must be "non-overlapping" in time.

Contemporaneous extrinsic evidence describing OLED circuits confirms that they select only one scan line at a time. One reference, in describing active matrix LCD and OLED circuits, states that "[o]nly one scan line is selected at a time." Ex. BB03 at 50-52. Another reference describing a matrix of OLED pixels states that "each Vselect row [of pixels connected to a

selection scan line is] selected *in turn*." Ex. BB04 at DEFS_CC_4371. Both the intrinsic and extrinsic evidence thus support HP's construction that "selection periods" cannot overlap.

D. "designating current" (Claim 1)

Solas's Proposal	HP's Proposal
Plain and ordinary meaning, *i.e.*, current designating a value corresponding to an image signal	"current corresponding to an image signal having a specified current value that is held constant"

The parties agree that "designating current" is a current corresponding to an image signal, but dispute whether the value of that current must be held constant. HP proposes that the value of be held constant based on the specification's express statement and the fact that the '042 Patent uses a "current programming" technique that requires a constant current. Solas's proposal, meanwhile, encompasses prior art "voltage programming" techniques that the patent disparages.

As background, the "designating current" is a current applied to the current lines that effectively determines the brightness of OLED pixels. '042 at 11:41-63. The '042 Patent consistently refers to the "designating current" using a variable "$I_{DATA.}$" *See, e.g.*, *id.* at 4:26-32, 11:41-63. The specification expressly states that I_{DATA} is generated by the current source driver, which "*holds the current value of the tone designating current* I_{DATA} *constant* in a period from the end of each reset period T_R to the end of the corresponding selection period T_{SE}." *Id.* at 11:41-63.

Solas's proposal not only disregards the specification's express statement, it also attempts to broaden the claims onto prior art "voltage programming" driving methods. "Voltage programming" systems are controlled by a designating, constant voltage, as opposed to a designating, constant current. Kanicki Decl. ¶35. The '042 Patent disparages such voltage programming systems, noting that systems "in which the luminance and tone are controlled by the *signal voltage*, it is difficult to uniquely designate the current value of an electric current which flows through the organic EL element." '042 at 2:11-28. This causes "the luminance of the

organic EL element [to] change[] from one pixel to another" and "produces variations in luminance on the display screen." *Id*. According to the '042 Patent, prior art "voltage programming" systems, unlike the "current programming" system disclosed in the '042 Patent, cannot compensate for the disparate properties of individual transistors, which change "in accordance with a change in ambient temperature, or … when the transistor is used for a long time." *Id.* The court should therefore adopt HP's construction that properly excludes disparaged prior art "voltage programming" systems with varying designating current levels from the scope of the claims.

E. "current lines" (Claim 1)

Solas's Proposal	HP's Proposal
Plain and ordinary meaning, *i.e.*, conductive lines for carrying current	"conductive lines, each connected to a plurality of pixel circuits and carrying current"

HP's construction clarifies that "current lines" each carry current to a "*plurality* of pixels circuits" rather than only *one* pixel circuit as Solas's proposal permits. HP's construction follows from the specification, which defines "current lines" as the parallel "Y" lines (red) in Figure 3 below running in the column direction that supply the designating current from the current source driver to the pixel circuits. '042 at 4:22-32, 5:10-21. Each current line connects to a column of multiple pixel circuits, with each pixel circuit labeled "P" and annotated in blue. *Id.* at 5:10-20, 5:31-35, 5:50-54. There is no disclosure supporting Solas's contention that a current line could connect to only one pixel circuit. Indeed, such a disclosure would be fundamentally at odds with the structure of OLED display

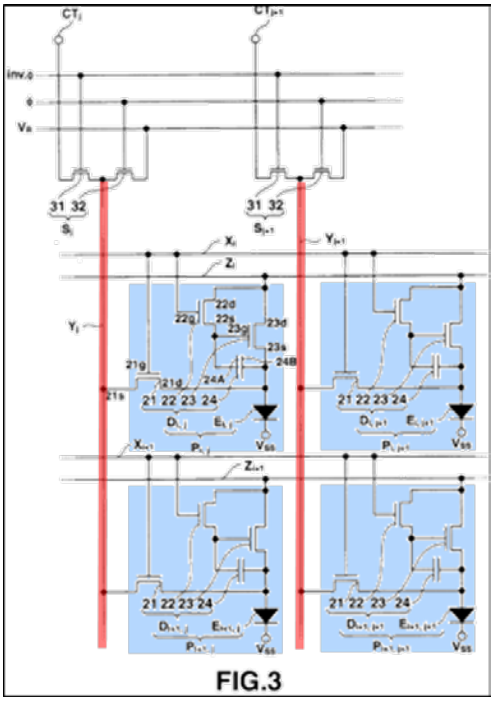


FIG.3

panels, which have thousands or millions of pixel circuits arranged in columns (connected to "current lines") and rows (connected to "selection scan lines").

Solas's proposal, "conductive lines for carrying current," is also flawed because it renders "current lines" meaningless as every "conductive line" is used for "carrying current." Yet the specification and claims are clear that there are other types of "conductive lines" — "selection scan lines," "supply lines," and lines inside each pixel circuit — that carry current, but are distinct from the "current lines." Because no disclosure in the '042 Patent suggests "current lines" could encompass any line carrying current, Solas's proposal should be rejected.

III. U.S. Patent No. 7,663,615 ("'615 Patent")

A. '615 Patent Background

The '615 Patent is directed to an OLED pixel circuit shown in Figure 1 (annotated to the right) that includes a "light emission drive circuit DC" (box labeled "DC") connected to an "organic EL element" (labeled "OEL" in yellow). '615 at 17:7-9, 17:32-35. The "light emission control drive circuit DC" comprises four parts: (i) a "capacitor (electric charge accumulating means and a capacity element) Cs" (orange); (ii) a "drive transistor (light emission control means) Tr13" (green); (iii) a "selection transistor (writing control means) Tr12" (purple); and (iv) "holding transistor (voltage control means) Tr11" (blue). *Id.* at 17:7-31. These parts are connected to and controlled by three types of lines: (i) "data lines DL" (red); (ii) "selection lines SL" (purple); and (iii) "hold lines HL" (blue). *Id.* The only asserted independent claim,

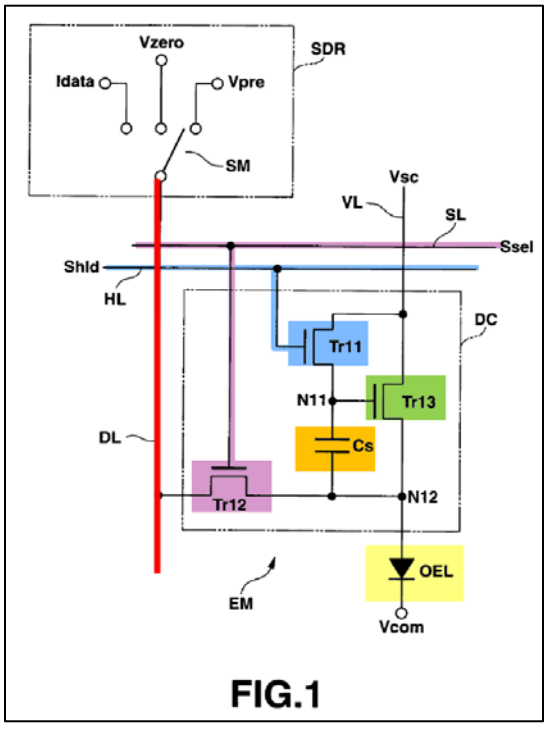


FIG.1

Claim 11, recites a "display unit" comprising various "elements," "sections," and "lines." Each of these components correspond to one of the parts in Figure 1 as summarized in the table below.

Structure Recited In Claim 11	**Corresponding Part In Specification (annotated color in Fig. 1)**
"light emission element"	"organic EL element" ("OEL") (yellow)
"light emission drive circuit"	"light emission drive circuit DC"
"electric charge accumulating section"	"capacitor (electric charge accumulating means and a capacity element) Cs" (orange)
"light emission control section"	"drive transistor (light emission control means) Tr 13" (green)
"writing control section"	"selection transistor (writing control means) Tr 12" (purple)
"voltage control section"	"holding transistor (voltage control means) Tr 11" (blue)
"selection lines"	"selection lines SL" (purple)
"hold lines"	"hold line HL" (blue)
"data lines"	"data lines DL" (red)

B. "the operation" (Claim 11)

Plaintiff's Proposal	**HP's Proposal**
"generating a light emission drive current having a predetermined current value in accordance with the electric charges accumulated in the electric charge accumulating section and supplying the light emission drive current to the light emission element"	Indefinite

The term "*the* operation" lacks antecedent basis and renders the asserted claims indefinite. The term appears in Claim 11's element, "a voltage control section for controlling a drive voltage for making the light emission control section perform the operation." But no other part of Claim 11 recites any "operation" or other phrase corresponding to "the operation." Kanicki Decl. ¶56.

A claim is indefinite if it recites a "term [that] does not have proper antecedent basis where such basis is not otherwise present by implication or the meaning is not reasonably ascertainable." *Halliburton Energy Serv., Inc. v. M-I LLC*, 514 F.3d 1244, 1249 (Fed. Cir. 2008). Applying this principle in *Cellular Communications Equipment LLC v. AT&T, Inc.*, a court found the term "the apparatus" lacked any explicit or implicit antecedent basis, particularly when it was part of a claim that recited transmission between "one apparatus to another." No. 2:15-CV-576-RWS-RSP, 2016

WL 7364266, at *8-9 (E.D. Tex. Dec. 19, 2016). And in *Image Processing Technologies, LLC v. Samsung Electronics Co.*, a court found claims indefinite because they recited "the boundary," but either provided no antecedent basis at all or recited four types of "boundaries," making it "unclear [as to] which of the referenced four boundaries of the target is referred to by the phrase 'the boundary.'" No. 2:16-cv-505, 2017 WL 2672616, at *32 (E.D. Tex. June 21, 2017).

Further, here, the lack of antecedent basis for "the operation" is only worsened by the '615 Patent specification, which refers to at least seven different types of named "operations" — (1) "precharge operation"; (2) "threshold correction operation"; (3) "writing operation"; (4) "light emission operation"; (5) "display operation"; (6) "graduation sequence display operation"; (7) "drive control operation"; and also just "operation" generically. '615 at 18:37-19:9 (summarizing five of the different types of "operations"), 23:20-26 (describing "gradation sequence display operation), 27:9-15 (using "display operation"); *see also id*. at 1:60-63, 23:27-33 (using just "operation"). It is impossible for a person of ordinary skill to determine which one, many, or none of these "operations" is "the operation" in the claims. Kanicki Decl. ¶¶54-63.

Solas proposes to remedy the lack of antecedent basis by rewriting the claim and replacing "the operation" with a 36-word phrase. But it is unclear why "the operation" should refer to the phrase Solas proposes, particularly when that phrase includes two separate "operations" of "generating a light emission drive current" and "supplying the light emission drive current." At any rate, a district court can correct a patent only if (1) the correction is not subject to reasonable debate based on consideration of the claim language and the specification and (2) the prosecution history does not suggest a different interpretation of the claims. *Novo Indus., L.P. v. Micro Molds Corp.*, 350 F.3d 1348, 1357 (Fed. Cir. 2003). Under this standard, courts have refused to correct antecedent basis deficiencies if the correction addresses "more than a misspelling or a missing

letter" or an "obvious clerical error." *Smith v. ORBCOMM, Inc*., No. 2:14–CV–666, 2015 WL 5302815, at *12 (E.D. Tex. Sept. 10, 2015); *Smartflash LLC v. Apple Inc.*, 77 F. Supp. 3d 535, 560-61 (E.D. Tex. 2014). Here, Solas's insertion of 36 words far exceeds a minor correction.

C. "precharge voltage" (Claim 11)

Plaintiff's Proposal	**HP's Proposal**
Plain and ordinary meaning	Indefinite

The term "precharge voltage" renders the asserted claims indefinite because the '615 Patent specification describes two types of "precharge voltages," and it is impossible for a person of ordinary skill to determine which (if any) of these two is referenced in the claim. Claim 11 only exacerbates the ambiguity by reciting a single "precharge voltage" that has characteristics of *both* types of "precharge voltages" in the specification — an absurd outcome given that the specification's two types of "precharge voltages" are entirely distinct and have critical differences.

Claim 11 uses the term "precharge voltage" in the following limitation: "the data driver applies a *precharge voltage* exceeding a threshold value of the drive transistor to the data line." According to this limitation, the same single "precharge voltage" has two characteristics: (1) it is applied by the "data driver" to the "data line" and (2) it has a value that "exceed[s] a threshold value of the drive transistor." Kanicki Decl. ¶72. The problem, however, is that there is no such "precharge voltage" in the '615 Patent that has *both* recited characteristics. Instead, the '615 Patent specification describes two distinct types of "precharge voltages":

(1) A "precharge voltage" called "Vpre," which is applied to the "data line" as recited in Claim 11, but could be *less* than the threshold voltage of a drive transistor;

(2) A distinct "precharge voltage" called "Vpre13," which exceeds the threshold voltage of a drive transistor as recited in Claim 11, but is *not applied* to the "data line."

These distinctions between the two types of precharge voltages are explained in annotated Figure 3A, with Vpre in red and Vpre13 in blue. The two precharge voltages first differ in *where* they are applied. Vpre is applied on a "data line," the vertical red line in Figure 3A. As the specification states: "*precharge voltage Vpre* [is] to be *applied to the data line DL* from the signal drive circuit SDR." '615 at 20:44-49; *see also id*. at 19:44-47; Kanicki Decl. ¶65-68, 73. By contrast, Vpre13 is not applied to the data line (in red). Rather, Vpre13 is "applied to the opposite ends of the capacitor Cs." *Id*. at 20:63-67. That is, Vpre13 is applied across the capacitor "Cs," labeled in blue. Kanicki Decl. ¶65-68, 73.

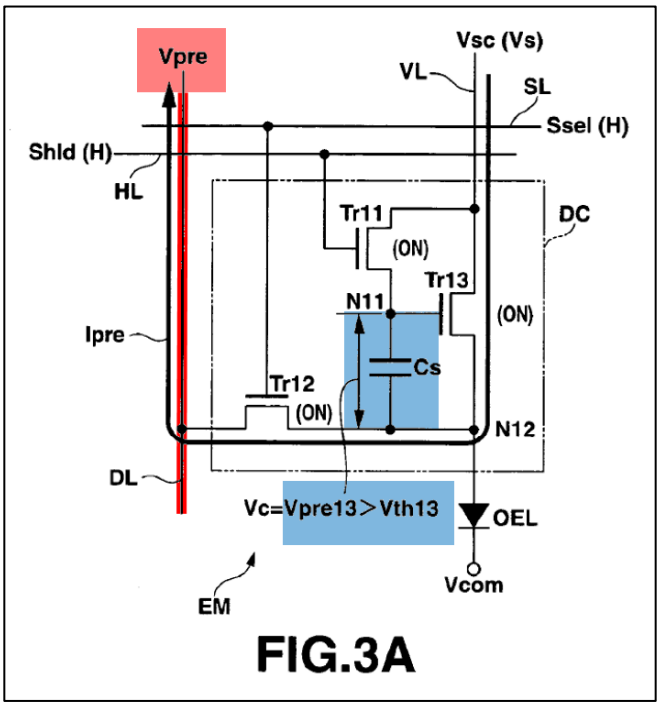


FIG.3A

The two precharge voltages also differ in their voltage *values*. Vpre13's value must be *greater* than the threshold value of the drive transistor, Vth13. Kanicki Decl. ¶69. As Figure 3A states, "Vpre13 > Vth13." The specification confirms repeatedly, stating the precharge voltage "*Vpre13 that is larger than the threshold Vth13* of the drive transistor Tr 13 is applied to the opposite ends of the capacitor Cs" and "the voltage *Vpre13 is higher than the threshold voltage Vth13*." '615 at 19:7-9, 20:63-67. By comparison, the specification places no such requirement on Vpre's value. It provides only one equation below regarding Vpre's value, which places no requirement on Vpre being greater than Vth13. Kanicki Decl. ¶¶70-71.

"$|Vs-Vpre| > Vth12+Vth13 \qquad (1)$" (*Id*. at 20:49.)

On comparable facts in *Teva Pharmaceuticals v. Sandoz*, the Federal Circuit found the term "molecular weight" indefinite because it could refer to any one of three different weights called "Mp," "Mn," or "Mw" described in the intrinsic record. 723 F.3d 1363, 1368-69 (Fed. Cir. 2013). "Precharge voltage" is indefinite for similar reasons. The specification describes two distinct "precharge voltages," Vpre and Vpre13, each applied to a different part of a circuit and each having a different value. Yet Claim 11 confuses the two by reciting a single "precharge voltage" that both (1) is applied to the "data line" and (2) "exceed[s] a threshold value of the drive transistor." Because it is impossible to determine which of the two "precharge voltages" in the '615 Patent is being referenced by Claim 11's "precharge voltage," the claim is indefinite.

D. "writing control section" (Claim 11)

Plaintiff's Proposal	**HP's Proposal**
Plain and ordinary meaning, *i.e.*, circuit section that controls writing	"a transistor that controls the writing of both the gradation sequence signal and the precharge voltage from a data line to the charge accumulating section"

As explained in Section III.A, Claim 11 recites four distinct "sections" and each "section" references one of the components in the specification's Figure 1. Consistent with the structure and functions that patent attributes to the "writing control section," HP proposes construing the term as "a transistor that controls the writing of both the gradation sequence signal and the precharge voltage from a data line to the charge accumulating section." Solas's proposal of "circuit section that controls writing" is wrong because it erases any distinction between the "writing control section" and the other "sections" recited in the claim, each of which also "controls writing."

The "writing control section" corresponds to a "selection transistor Tr 12" in the specification, labeled in purple in Figure 1 in Section III.A and Figures 3A and 3B below. Indeed, the specification refers to Tr12 both as the "selection transistor" and the "writing control means": "As shown in FIG. 1 . . . a light emission drive circuit DC according to the invention is configured

so as to have: *a selection transistor (writing control means) Tr 12*." '615 at 17:7-9. Thus, the "writing control section" is "a transistor" as in HP's proposal.

The functions that the specification attributes to transistor Tr12 match the two functions that Claim 11 attributes to the "writing control section." First, Claim 11 recites that the "light emission drive circuit *applies the precharge voltage* applied to the data line to the electric charge accumulating section *via the writing control section*." Thus, the "precharge voltage" is applied between the "data line" and "charge accumulating section" (*i.e.*, capacitor) "via the writing control section." This matches annotated Figure 3A, which shows that when transistor Tr12 (purple) is turned on, the "precharge voltage Vpre" is applied between the data line (red) and the capacitor Cs (orange) "via" the transistor Tr12. The specification confirms, stating: "selection transistor Tr 12 is turned on and the data line DL to which the *precharge voltage Vpre is applied* electrically communicates with . . . the capacitor Cs (the contact point N12) *via the selection transistor Tr 12*." *Id*. at 20:36-43.

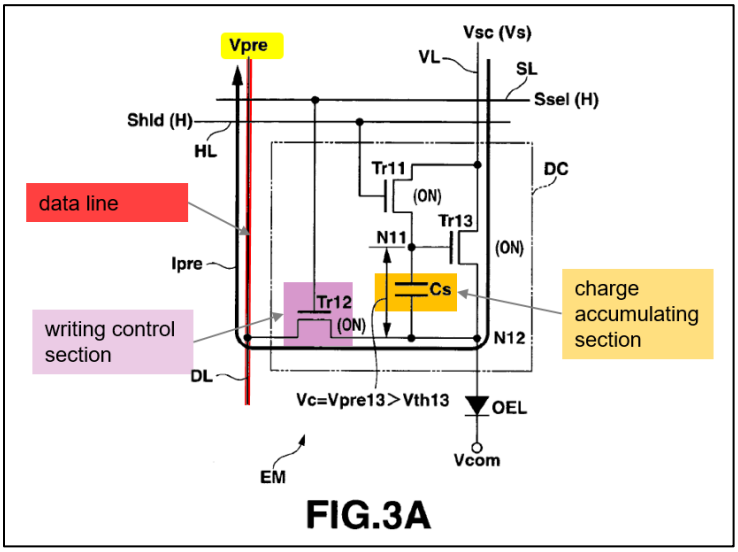


FIG.3A

Second, Claim 11 recites the "*writing control section* [is] for controlling a supplying state of the electric charges based on the *gradation sequence signal* to the electric charge accumulating section." The "writing control section" thus controls whether to write the "gradation sequence signal" to the "charge accumulating section." This matches Figure 4A, which shows that when Tr12 (purple) is turned on, a "gradation sequence current *Idata*" flows between the data line (red) and capacitor Cs (orange) "via" the transistor Tr12. The specification confirms, stating: "gradation

sequence current Idata flows . . . *via* the drive transistor Tr 13, the contact point N12, the *selection transistor Tr 12, and the data line DL*." *Id*. at 24:5-11. In sum, the transistor Tr12 acts as an on/off switch that controls the writing of both the precharge voltage and gradation sequence signals. These functions match the functions of the "writing control section" in Claim 11.

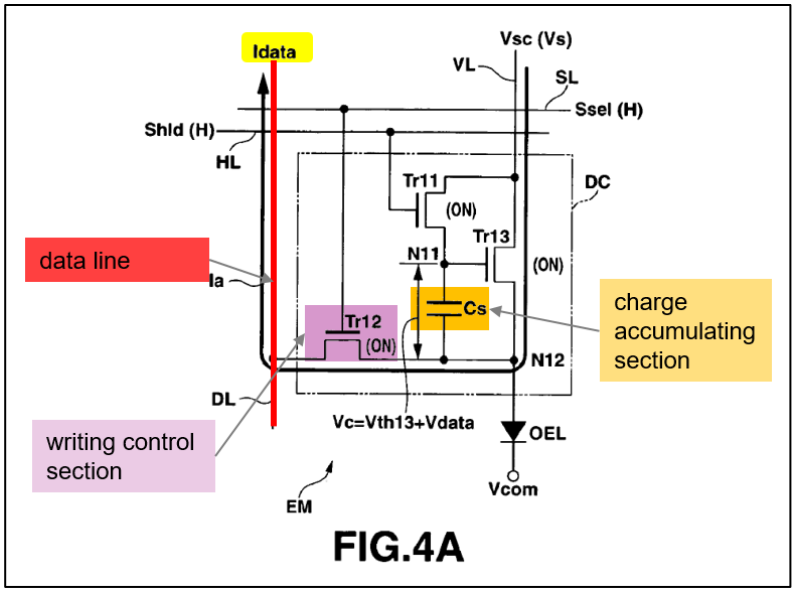


FIG.4A

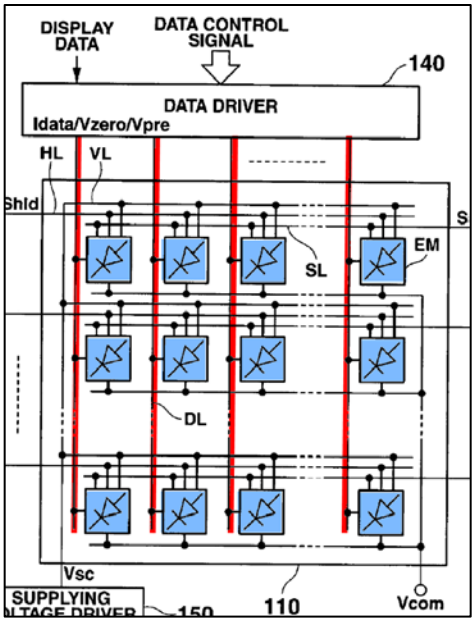
Solas's definition of "circuit section that controls writing," meanwhile, is flawed because it does not specify *what* is being written and, as a result, could describe any of the other "sections" in Claim 11, which also control writing. In Claim 11, the "light emission control section" controls writing of a "light emission drive current" and the "voltage control section" controls writing of a "drive voltage." Thus, only HP's construction gives "writing control section" a meaning that is consistent with the intrinsic record while Solas gives the term virtually no meaning at all.

E. "data lines" (Claim 11)

Plaintiff's Proposal	**HP's Proposal**
"conductive lines for supplying information"	"conductive lines, each connected to and carrying data to a plurality of light emission drive circuits"

The parties agree that "data lines" are "conductive lines," but dispute whether each "data line" (1) connects to "a plurality of light emission drive circuits" (as HP proposes) or (2) can connect to *only* one "light emission drive circuit." (as Solas proposes). HP's construction follows from '615 Patent's consistent disclosure. For example, Figure 16 depicts the "entire structure of a display unit" with multiple "data lines" DL. Each data line connects to one column of a plurality

of "display pixels" EM (blue), where each display pixel includes a "light emission drive circuit." Figure 16 thus illustrates "display panel 110 arranged in a matrix composed of n rows x m columns . . . of plural display images provided with the light emission drive circuit DC" and "plural data lines DL arranged in a column direction." '615 at 34:52-62.



Solas's proposal is incorrect as it permits each "data line" to connect to only *one* light emission drive circuit. There is no such embodiment or disclosure in the specification. Any such disclosure would be fundamentally at odds with the structure of OLED display panels, which typically have millions of pixel circuits across thousands of columns, each connected to a data line.

HP's construction also correctly defines the function of "data lines" as carrying "data." This function follows from the plain meaning of the term itself, "*data* lines," and the specification, where Figure 16 above shows that the data lines carry signal values supplied by a "data driver" 140 based on "display data." *Id*. at 35:2-10. Solas's proposal's use of "information" is incorrect to the extent "information" has a meaning different or broader than "data."

IV. U.S. Patent No. 7,573,068 ("'068 Patent")

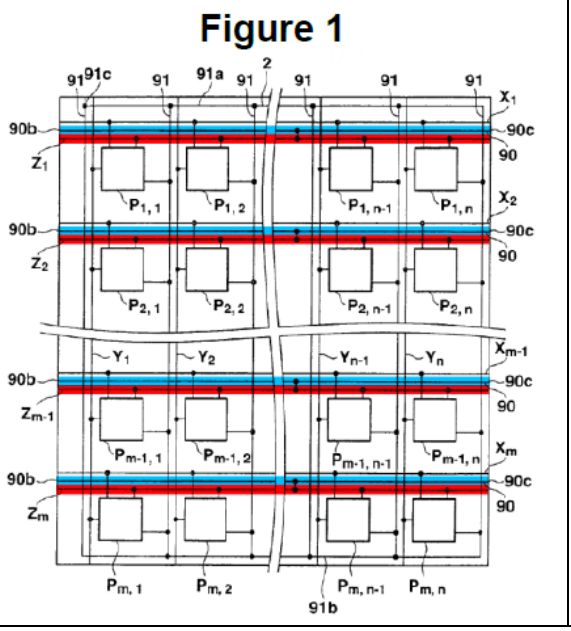
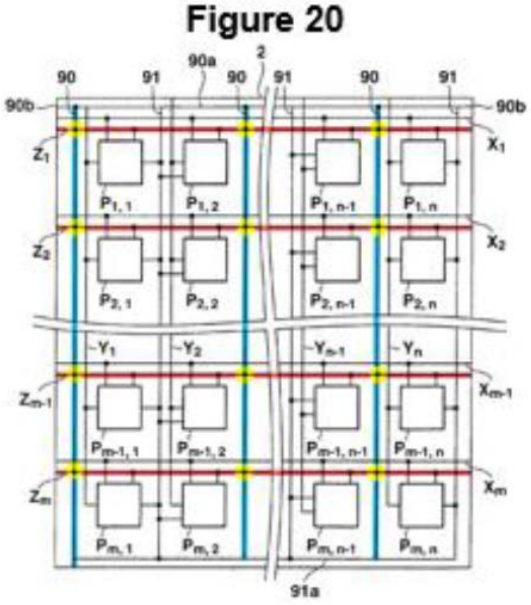
A. "formed on said plurality of supply lines along said plurality of supply lines" (Claim 1) / "connected to said plurality of supply lines along said plurality of supply lines" (Claim 13)

Plaintiff	Defendants
"formed on said plurality of supply lines over the length or direction of said plurality of supply lines"	"stacked on or making multiple contacts with said plurality of supply lines over the length of each supply line"
"connected to said plurality of supply lines over the length or direction of said plurality of supply lines"	

The '068 Patent's purported invention is to reduce the resistance of supply lines by forming thick "feed interconnections" on top of the supply lines, which helps address problems known as "voltage drops" and "signal delays." *See, e.g.*, '068 at 2:39-41, 4:4-14. The disputed terms pertain to how the feed interconnections are physically "formed on" or "connected to" the supply lines to achieve those objectives, and appear in the phrases: "a plurality of feed interconnections which are formed on said plurality of supply lines along said plurality of supply lines" (Claim 1) and "a plurality of feed interconnections which are connected to said plurality of supply lines along said plurality of supply lines" (Claim 13). The '068 Patent discloses only two ways to "form" or "connect" the feed interconnections to the supply lines: (1) stacking the feed interconnection on top of the supply line over the length of the supply line, or (2) a grid formation in which the feed interconnections make multiple contacts with a plurality of supply lines over the length of each supply line. Defendants' construction accurately reflects these two disclosures. Solas's constructions, in contrast, are impermissibly broad, encompassing an arrangement where a supply line has only a single contact with one feed interconnection. The '068 Patent does not enable any such embodiment, and, as Solas's expert has admitted, an embodiment of that sort contravenes the purported objectives of the '068 Patent. Thus, Defendants' construction should be adopted.

The first of two disclosures in the '068 Patent teaches stacking the feed interconnection directly on top of the supply line, as seen in Figure 1, on the left below. In Figure 1, the feed interconnections (blue) are stacked on top of and in parallel to the supply lines (red), connecting the "feed interconnections" "over the length" of each supply line. '068 at 3:62-63 ("feed interconnections are stacked on the supply lines"), 6:2-4 ("The feed interconnections 90 are provided in parallel to the supply lines Z1 to Zm."). Stacking the feed interconnection over the length of the supply line achieves the alleged goal of the '068 Patent of reducing resistance in the

supply lines, decreasing signal delay, and suppressing voltage drops. *Id*. at 4:12-14. Defendants' construction accounts for this first disclosure with the following language: "stacked on . . . said plurality of supply lines over the length of each supply line."

'068, Figure 1 (first embodiment)	**'068, Figure 20 (second embodiment)**
	

The second disclosure in the '068 Patent, seen in Figure 20 on the right above, teaches a "grid" formation between the plurality of feed interconnections (blue) and plurality of supply lines (red), which run in perpendicular directions, resulting in the feed interconnections crossing each supply line at multiple contact points (yellow dots). *Id*. at 23:1-3 ("The feed interconnections 90 are connected to the supply lines Z1 to Zm and branched in parallel to the signal lines Y1 to Yn when viewed from the upper side."). The second disclosure achieves the stated goal of the '068 Patent of reducing the resistance in the supply lines by connecting multiple low-resistance feed interconnections to multiple supply lines, thereby decreasing resistance across the entire "grid" of connections. Importantly, nowhere in the '068 Patent does it disclose that a supply line with only a single contact to one feed interconnection would suffice to practice the claimed invention.

Defendants' construction accounts for this second disclosure: ". . . making multiple contacts with said plurality of supply lines over the length of each supply line."

The parties agree that the '068 Patent discloses two ways to form or connect the feed interconnections to the supply lines. *See, e.g.*, Ex. DD01 at ¶¶ 28-31 (Solas's expert opining that "the patent discloses two relevant embodiments"). The parties also agree that the '068 Patent's first disclosure requires the feed interconnection to be formed "over the length" of the supply line—as reflected in the parties' proposals. The parties further agree that the construction of the disputed terms needs to reflect the second "grid" disclosure. Where the parties disagree—and where the dispute lies—is how the constructions should account for the second "grid" disclosure.

Defendants' construction accurately captures the "grid" disclosure by requiring multiple contacts between each feed interconnection and each supply line, over the length of each supply line. Solas attempts to capture the "grid" disclosure using the phrase "over the . . . direction of said plurality of supply lines." But that phrase renders Solas's constructions both ambiguous and overbroad. First, it is unclear what it means for a feed interconnection to be formed on or connected "over the *direction* of said plurality of supply lines." Second, Solas's constructions go well beyond the teachings of the '068 Patent, as it could encompass an embodiment with a supply line having only a *single* contact with one feed interconnection. But, as discussed above, the '068 Patent does not disclose or enable any such embodiment. Constructions broad enough to include such an embodiment would render the claim invalid for lack of enablement. *Trustees of Bos. Univ. v. Everlight Elecs. Co.*, 896 F.3d 1357, 1365 (Fed. Cir. 2018) (invalidating patent claim because plaintiff's broad claim construction did not enable the full scope of the claim). For that reason alone, Solas's constructions should be rejected. Moreover, in Solas's related action against LG Display, Solas specifically disavowed the possibility of a single point of contact, representing that

it "does *not* contend that 'along' covers something that is 'formed on' or 'connected to' *only at a single 'arbitrary point.'*" Ex. DD02 at 11 (emphasis added).

Solas's construction should also be rejected because permitting a supply line to make a single contact with only one feed interconnection would defy the overall objective of the '068 Patent. Claims should be construed in a manner that "achieve[s] the overall object of the invention," and constructions "in tension with . . . the objectives of the [patent] as expressed in the specification and the prosecution history" should be rejected. *Praxair, Inc. v. ATMI, Inc.*, 543 F.3d 1306, 1324 (Fed. Cir. 2008). Here, the '068 Patent's stated objective and its reason for having feed interconnections at all is to allegedly improve the conductivity of the supply lines and avoid prior art problems of voltage drops and signal delays. *See* '068 at 4:24-35 ("interconnection can suppress the voltage drop"), 18:26-40, 26:62-66. These objectives can only be met if the feed interconnections and supply lines are stacked or have multiple contacts over their lengths. Indeed, Solas's own expert has admitted that having only a single contact between a supply line and a feed interconnection would not achieve the '068 Patent's objective. He testified that if the feed interconnection and supply lines connected only at one point, "you would expect a voltage drop and a signal delay," which is contrary to the "purpose of the [feed interconnections, which] is to reduce the voltage drop." Ex. DD03 at 213:19-215:10. Despite Solas's expert's statements that a supply line making a single contact with only one feed interconnection would fall outside the scope of the claims, Solas's proposed construction provides no guidance to that effect—only Defendants' construction does. Defendants' construction should therefore be adopted.

B. "signal lines" / "supply lines" (Claims 1, 13)

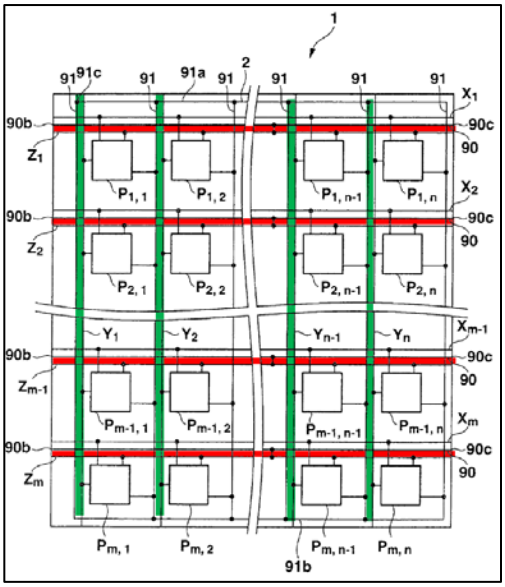
Term	Plaintiff	Defendants
"signal lines"	"conductive lines supplying signals"	"conductive lines carrying data"
"supply lines"	"conductive lines supplying current or voltage"	"conductive lines, each supplying a driving current or voltage to a plurality of pixel circuits"

The '068 Patent describes two distinct conductive lines: "signal lines," and "supply lines." The two types of lines have distinct structures and functions in the operation of an OLED pixel and are not interchangeable. Defendants' constructions recognize these distinctions, and reflect the '068 Patent's specific disclosures regarding each type of line. In contrast, Solas's constructions erase any distinction between the two types of lines, making them interchangeable, because in any circuit, every "signal" is represented as a "current or voltage."

"Signal lines" and "supply lines" are two different terms, and it is axiomatic that "different claim terms are presumed to have different meanings." *Helmsderfer v. Bobrick Washroom Equip., Inc*., 527 F.3d 1379, 1382 (Fed. Cir. 2008). The "signal lines" and "supply lines" have different functions and structures according to the '068 Patent. Each type of line carries a distinct type of current or voltage. The signal lines carry a "write current" corresponding to "data" for images to be displayed. The specification explains that "a *data* driver supplies a *write current* (current signal) to all the *signal lines* Y1 to Yn." '068 at 15:61-63 (emphasis added). In contrast, the supply lines supply a "driving current" that is a power supply, and do not carry data. The specification is clear that "the *driving current* flows from the feed interconnection 90 and *supply line* Zi . . . to the organic EL element" and a "*driving current* having a magnitude corresponding to the level of the gate voltage *is supplied from the power supply*." *Id*. at 1:41-44, 16:52-54 (emphasis added). In simple terms, the data written to the "signal line" instructs the pixel how bright to illuminate, and then the "supply line" supplies a driving current to illuminate the pixel as instructed. These are not interchangeable functions. Consistent with these disclosures, the constructions of "signal

lines" and "supply lines" should reflect, as Defendants' constructions do, that (1) "signal lines" carry "data," while (2) "supply lines" supply a "driving current or voltage."

Further, the two types of lines are distinct structures. In every embodiment, as seen for example in Figure 1, the supply lines (red) are depicted as distinct from the signal lines (green). There are no instances in which the '068 Patent refers to the signal lines and supply lines interchangeably. Moreover, as Figure 1 shows, each supply line supplies the driving current to a row of *multiple pixel circuits* ($P_{m,n}$). *See, e.g., id.* at 16:38-61; Figs. 1, 20. The supply lines are the only lines disclosed in the '068 Patent that provide a driving current to the plurality of pixel circuits, and there are no embodiments where a supply line connects to just one pixel circuit. *Id.*



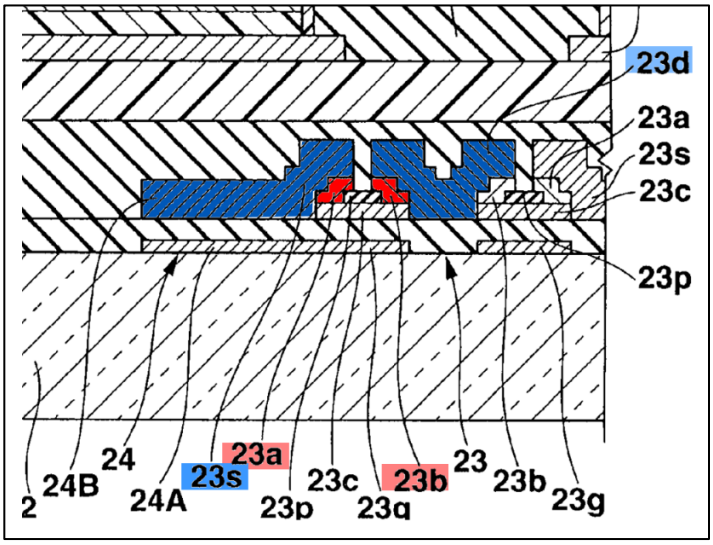
Whereas Defendants' constructions recognize the distinctions between signal and supply lines, Solas's proposals for the two terms are substantively identical: (1) "conductive lines supplying signals" (for "signal lines") and (2) "conductive lines supplying current or voltage" (for "supply lines"). There is no actual distinction between Solas's constructions because every "signal" in an electronic circuit is represented as a "current or voltage." As a result, Solas's construction for "supply lines" ("conductive lines supplying current or voltage") could just as easily define "signal lines" because all signals carried on the "signal lines" are in the form of a "current or voltage." For these reasons, Solas's proposed constructions should be rejected.

C. "source" / "drain" (Claims 1, 13)

Plaintiff	Defendants
Plain and ordinary meaning	"source electrode" / "drain electrode"

"[W]hen a patentee uses a claim term throughout the entire patent specification, in a manner consistent with only a single meaning, he has defined that term by implication." *Bell Atl. Network Servs., Inc. v. Covad Commc'ns Grp, Inc.*, 262 F.3d 1258, 1271 (Fed. Cir. 2001).

Here, the specification's consistent and exclusive usage of "source" and "drain" to refer to the conductive film "electrodes" demonstrates that the inventors intended to define those terms to mean "source electrode" and "drain electrode," respectively. In particular, Figure 5 (excerpted in relevant part) depicts a driving transistor 23 with elements 23s and 23d (blue) formed on corresponding elements, labeled 23a and 23b, respectively (red). In describing Figure 5 and these elements, the specification states: "The *drain 23d* is formed on one impurity-doped semiconductor film 23a. The *source 23s* is formed on the other impurity-doped semiconductor film 23b." '068 at 8:64-66 (emphasis added). The "source" 23s and "drain" 23d are electrodes, as the specification states that they are made of a "conductive film" material: "the drains 23d and sources 23s . . . are formed, using photolithography and etching, by patterning a single *conductive film* formed on the entire surface of the gate insulating film 31." *Id.* at 9:36-44 (emphasis added). In other words, the specification explains that the "source" and "drain" formed from "conductive film" are formed on top of "impurity-doped semiconductor film." The inventors chose to refer to the conductive electrodes as "source" and "drain," demonstrating a clear intent to define the terms with that single meaning. *Bell Atl. Network Servs.*, 262 F.3d at 1271.



Solas's failure to provide a construction—instead proposing only plain and ordinary meaning—fails to account for the inventors' definition of those terms. In addition, adopting plain and ordinary meaning for these terms provides no guidance as to what structures within the driving transistor "source" and "drain" allegedly encompass. Indeed, during the meet and confer process, Defendants asked Solas what structures source and drain encompass, and Solas provided no response. This lack of clarity highlights why plain and ordinary meaning is inadequate here for "source" and "drain."

Although Solas provides no explanation for what it means by "plain and ordinary meaning," to the extent Solas contends that the plain and ordinary meaning is the "impurity-doped semiconductor film" upon which the electrodes are formed, such a construction should be rejected because it contradicts the inventors' express use of "source" and "drain" to refer only to conductive electrodes 23s and 23d. '068 at 8:64-66.[4] In contrast, the '068 Patent refers to elements 23a and 23b as "impurity-doped *semiconductor film*," (*id.* (emphasis added)) thus referring to semiconductor regions 23a and 23b of the driving transistor by a term *other than* "source" and "drain." The unambiguous distinction that the '068 Patent specification draws demonstrates that the inventors intended for the terms "source" and "drain" to mean "electrodes," not semiconductor films. Defendants' constructions correctly capture this intent.

[4] Several dictionary definitions are also consistent with the inventors' use of the terms "source" and "drain" to refer only to conductive electrodes. One dictionary describes both the "source" and "drain" as "usually considered to be the *metal contact* at the surface of the die," while two others define "source" as an "electrode." Exs. DD04 at 213, 643; Ex. DD05 at 644 (defining "source" as "[i]n a field-effect transistor, the *electrode* . . .."); Ex. DD06 at 737-38 (defining "source" as "[t]he *electrode* in a field-effect transistor . . .").

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Respectfully submitted:

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CERTIFICATE OF SERVICE

The undersigned certifies that on June 25, 2020, I electronically filed this document with the Clerk of Court via the Court's CM/ECF system which will send notification of such filing to all counsel of record, all of whom have consented to electronic service in this action.

/s/ Michael E. Jones